Proceedings of the 33rd European Safety and Reliability Conference (ESREL 2023)
Edited by Mário P. Brito, Terje Aven, Piero Baraldi, Marko Čepin and Enrico Zio
 Published by Research Publishing, Singapore.
doi: 10.3850/978-981-18-8071-1_P163-cd

Novel Implementation of an FPGA-based Real Time Impedance Spectroscopy for Highly Integrated Reliable Safety Systems

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The power supply of battery-based safety systems is a highly critical component due to its influence on all system functions. To guarantee functionality the state of the battery must be known at any time. Especially the current State of Charge (SoC) and State of Health (SoH) must be monitored continuously to guarantee functionality during deployment. It is not possible to fully discharge the battery of a system that needs to provide energy to perform safety functions. This makes current state of the art methods like Voltage Analysis (DVA) or Coulomb Counting (CC) unusable. This especially is a problem in subsea systems where components cannot be easily exchanged, and a design life of 25 years is common. A solution for this problem is the Electrochemical Impedance Spectroscopy (EIS) which can be conducted at any SoC. The EIS provides impedance values over a defined set of frequencies that correspond to different chemical processes which can be used to accurately estimate the battery state.
A novel real time EIS implementation is proposed which uses the on-board charger of the Battery Management System (BMS) to perform the measurement. No additional components are required as the EIS is calculated on a Field Programmable Gateway Array (FPGA) in real time which makes it useable for embedded systems. The structure of the impedance measurement system is presented, and the functionality of the embedded impedance spectroscopy is proven using an RC-circuit as a reference load.

Keywords: EIS, FPGA, Impedance, Real-Time, Reliability, Safety

1. Introduction

Safety critical and high reliable applications like subsea production systems [1], [2] require a reliable and safe power supply over the whole service life. This especially applies to the batteries that provide the energy for the system as they are complex electro-chemical systems that are exposed to variable loads and environmental conditions. To guarantee availability highly reliable and accurate diagnosis methods are needed, that can monitor the state of the battery. Even though this task can be overcome through the usage of 0CV analysis methods like differential Voltage Analysis or Incremental Current Analysis [3-4] there are special systems where those methods cannot be applied. In systems which need to perform an action to reach a safe state the amount of energy needed to perform this safety action always needs to be available. This is especially challenging in subsea systems where the system cannot be

accessed or tested externally and a long design life of 25 years without maintenance is required. Therefore, there is a need for an accurate battery State of Health (SoH) diagnosis method that can be used during idle state without significantly changing the amount of charge in the system.

To cope with these challenges the Electrochemical Impedance Spectroscopy (EIS) can be used, as the cells do not need to be discharged to measure the cell properties. In the EIS various impedance measurements are conducted at different frequencies by exciting the system with a sinusoidal voltage or current and measuring the resulting system response. Then the calculated impedance values can be used to parameterize an equivalent circuit model or for direct correlation to effects that can be monitored at the specific frequencies [4-7]. An overview of detectable phenomena is given by Lvovich [4]. It is shown that information about general degradation [5-6], the State of Charge (SoC) [7][9], and the SoH [8-9] can be gathered using this measurement method by evaluating the resulting impedance plots.

Even though EIS is intensively studied there is still no universal solution for analyzing systems with impedance-based measurements. The correlation of impedance data with SoC and SoH is influenced by complex chemical processes that often cannot be monitored fully. Especially in deployed systems additional system insight that is required for correct correlation is often not available. Conducting EIS is not trivial as apart from difficult correlation the measurement of the values is failure prone. The amplitude of the excitation signal should be as small as possible so that the system behaves nearly linearly. Larger amplitudes lead to incorrect measurement values due to the cell's nonlinear behavior [8]. Too small amplitudes cannot be captured accurately due to resolution issues and measurement noise.

Excitation can only contain full amplitudes. If not accurately terminated the signal contains partial periods which distort the signal making it unusable. Ideally EIS is conducted during idling without charging or discharging the battery. Through sinusoidal excitation around the idle state and the usage of full periods not net charge will be introduced into the system. This is not applicable in the currently developed system as only positive currents can be realized by the charger. Therefore, a DC offset is necessary to realize a sinusoidal excitation. The higher the offset the larger the error of the measurement due to a change in the SoC. The effect worsens through elongated measurement times. Longer measurements can be used to calculate an averaged impedance over several amplitudes. Therefore, a trade-off between SoC change and filtering capability must be made in the dimensioning of the analysis algorithm.

Microchips [11] and patents are already realized that can conduct or describe the implementation of EIS. Patents that concern this topic can be accessed through the DPMA under the patent group G01R 31/392. These systems either need an additional complex microchip or additional components for excitation and logging of values. This is undesirable for safety systems since this adds hardware and increases complexity of the system. Therefore, a Field Programmable Gate Array (FPGA) is used to realize the analysis algorithm. The FPGA is a free programmable processing unit where high speed and parallel computation can be realized through a combination of transistors and pre-determined function units. The Battery Management System (BMS), that is used during this research, uses a Cyclone V FPGA as its main processing unit. Through intel's NIOS ii softcore processors high level control and complex computations can be realized. As the NIOS processor is a classical microprocessor synthesized on the FPGA, high level control and function programming using C++ can be used to control system functions and to route and capture data.

This paper proposes a highly integrated real time impedance calculation algorithm, that is implemented on an FPGA, to allow accurate and parameterizable measurements during idle state. Furthermore, a high-level control structure is presented, which efficiently manages the EIS measurement and routing of the data.

2. Method

The technologies and procedures used in this publication are introduced with a focus on system level functionality. The implemented algorithm itself and the testbench are described, as they are the essential part of the system implementation and proof of concept testing.

2.1 EIS algorithm development

The signal generator needed for the on-board measurement is composed out of a sine generator and a parameterizable frequency generator. A period counter used for termination of the measurement is also implemented. The impedance calculation that can compute the impedance in real

time is triggered by the same enable signals as the sine and frequency generator. All signals are delay-balanced, which is required for realizing accurate computation and termination on the FPGA. Every function component is realized in VHDL which is used to generate the layout for an FPGA. For most code generation the MATLAB/Simulink HDL Code Generator is used as this greatly accelerates the development process. For compilation and timing analysis the Quartus Prime 18.0 lite IDE by Intel is used.

2.2 Verification testbench

The verification testbench is composed of a BMS, a RC-load and a standard voltage supply. The BMS is composed of a buck-boost converter (BB) used for charging, an output switch to control current flow as well as current and voltage sensors. For replication of this test the charger needs to be stable up to the desired excitation frequency and the sensors need to sample at least at double the frequency of the desired measurement signal. Analog filtering of the measurement signal is highly suggested but is not feasible in this project. Through measuring at higher sample rates digital filtering can be used to mitigate the effect of aliasing and other distortions. In this study a 16-bit Analog-Digital Converter (ADC) with 600 kSps sample rate is used. Calculations are conducted on the integrated Cyclone V FPGA. High level control and communication through the Modbus protocol is realized on the implemented NIOS ii softcore processors. Logging of data and final conversion is initially done with Signal-Tap and later with LabView. To verify the system functionality a first order RC-circuit is used. The exact part values are measured, and the resulting impedance plot is calculated. The accuracy of the measurement algorithm is tested against the ideal impedance plot.

3. Results

The following findings and concepts were achieved during research on this topic. Mainly the integration of the impedance calculation as well as the required high level control structure will be covered. System verification shows that the developed system is functional and can be used in proceeding studies.

3.1 Impedance algorithm

As mentioned in the previous chapter a sinusoidal signal is needed for system excitation. The required sinusoidal signal is not inherently available in digital systems and must therefore be approximated. Sine generation is realized with a lookup table approach. The number of required logic elements is reduced by only saving a quarter of the full sine values. Through adaptation of the reference counter, that determines which value of the sign is put out, a full sine can be generated [10]. For the quarter wave an 8-bit resolution is deemed sufficient as the sine resolution will exceed measurement resolution after scaling.

Frequency modulation is realized by putting another slowdown-counter before the sine reference counter. By only incrementing the sine-reference counter after the slowdown-counter overflows the frequency can be controlled regardless of the FPGA base clock. By using a programmable 18-bit limit for the counter, the increments can be slowed allowing a frequency range from 1 Hz up to 200 kHz. Sine generation stops when the period counter reaches its determined limit. This also terminates the impedance measurement ensuring that no additional samples distort the calculated impedance value.

The same counter is also used for cosine generation which is needed for impedance calculation.

Impedance calculation itself is implemented by using the Discrete Fourier Transformation (DFT). By using the Euler-formula the DFT of the measured signal can be calculated from the measured values x(n), depending on the frequency factor k, with the following equations.

$$x(k)_{re} = \sum_{n=0}^{N-1} x(n) * \cos\left(2\pi * \frac{k*n}{N}\right) \quad (1)$$

$$x(k)_{im} = \sum_{n=0}^{N-1} x(n) * -\mathrm{j}\sin\left(2\pi * \frac{k*n}{N}\right) \quad (2)$$

Sine and cosine needed for real and imaginary part calculation are reused from the excitation module to minimize logic element usage. The calculation for real and imaginary parts of the voltage and current signal is split into four calculations that can be implemented with a singular recursive adder and only minimal additional logic. Usually when a Fourier Transformation is calculated a spectroscopy is conducted which evaluates the

frequency components of a sample. In the DFT application of this study, the phase and amplitude difference of only the set measurement frequencies is important. Therefor the real time single frequency is ideal for the use case as it only computes the impedance at the desired frequency. Through averaging over several measurement periods, a filtered impedance value is calculated, making the measurement less prone to external distortion. The number of periods depends on the measurement frequency and the signal amplitude.
Averaging can be efficiently implemented by summing up the single values and shifting the result to the right. This requires the number of periods p to be equal to 2^N where N is a natural number. To calculate the impedance of the system a complex division of current and voltage is conducted. The result is the unscaled impedance value. Division apart from shifting, especially using larger numbers, cannot be efficiently realized. Therefore, scaling of the measurement and complex division of the measured impedance values is not realized on the system hardware.
The designed algorithm is successfully implemented on the Cyclone V FPGA. The complete algorithm only uses 1455 logic elements, 1563 combinational ALUT units and four DSP blocks. Due to the small resource usage the system can possibly be implemented on smaller FPGAs.

3.2 Verification of the system

Measurements of the impedance are conducted with the fully integrated system. Each test frequency is measured several times to study accuracy and precision of the measurements. Furthermore, the required number of periods for capturing accurate impedance data is investigated.

Table 1. Impedance Standard deviation

Frequency [Hz]	Avg. RE Impedance	Std. Dev. RE Imp.	Avg. IM Impedance	Std. Dev. IM Imp.
1	5,407615273	0,00156199	-0,009593009	0,001616106
5	5,407780977	0,002099073	-0,054214159	0,001470827
20	5,390740665	0,000910889	-0,21698531	0,00252526
50	5,317083515	0,000915667	-0,521537627	0,000693542
100	5,104120788	0,001138935	-0,961988852	0,000431
200	4,507086892	0,001073765	-1,551279248	0,000547176
400	3,359053748	0,000670496	-1,845285375	0,000510285
800	2,298209477	0,002194286	-1,440216444	0,002223095
1000	2,077997615	0,000236781	-1,23559117	0,000348577

The verification measurements show very high repeatability indicating a stable measurement procedure. The accuracy of the measurement increases if the number of periods is increased. The accuracy of low frequency measurements does not improve significantly while increasing the number of amplitudes. Higher frequency measurements benefit from a larger number of measurement points. The reason for this is the reduced number of samples per measurement period as the ADCs always sample at the maximum stable conversion speed. As longer measurement times inflict a larger influence on the steady state the number of samples should be as low as possible. The verification measurements that are conducted show a constant deviation from the ideal RC-Circuit. This is identified to be a previously unidentified current branch in the system.

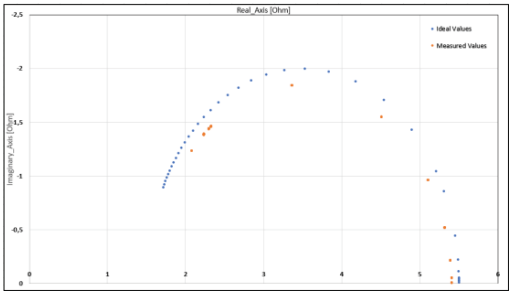

Figure 1. Reference measurement uncompensated

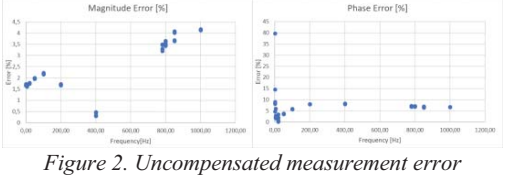

Figure 2. Uncompensated measurement error

After calibrating the measurement by approximating the impedance error through a quadratic function in relation to the measurement frequency the absolute error is significantly reduced. The resulting absolute deviation and measurement error is displayed in the following graph.

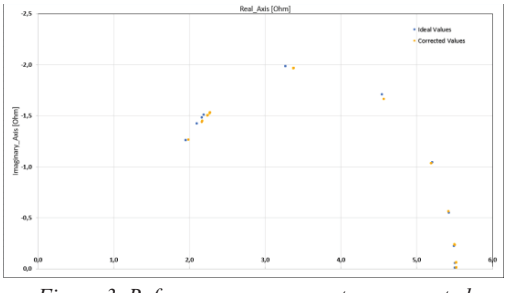

Figure 3. Reference measurement compensated

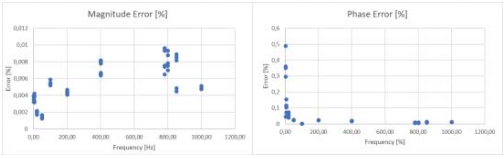

Figure 4. Compensated measurement error

4. Discussion

The measurements displayed in chapter three show excellent accuracy with ideal precision. Even without analogue filtering accurate results are achieved. The displayed results and documentations of logic element usage proofs that the system can be efficiently integrated into embedded systems. Design of the control loop will not be negatively affected through integration of the impedance measuring algorithm. The number of logic elements required is low enough that the system can be conveniently integrated into FPGA applications. The measurement accuracy is high enough to detect expected impedance deviations when compared to currently available impedance data in literature.

Through the integrated approach, which can measure the impedance at any desired SoC or SoH, the system state can be monitored at any point of interest, hugely increasing detectability and diagnostic coverage. Through external parameterization the system can be adapted after deployment to account for unpredicted ageing phenomena, which is especially important in dynamic chemical systems. This separates the system from previous publications, which often focused on equivalent circuit modelling, that heavily depend on the ageing factors that were simulated during the gathering of data.

The modular structure of the system can be extended by duplicating the impedance calculation unit without the need for additional external VHDL design. By adapting sine resolution and frequency counter the system can be adapted to other use cases. Through delay balancing of the signals between the modules accurate termination of the measurement is achieved. The verification of the system is used for an initial proof of concept. Full verification with battery cells is still ongoing. The used BMS is currently being investigated to remove leakage current and the resulting approximation of the measured error. A general calibration is still suggested to account for tolerances in the measurement electronics.

5. Conclusion

A novel implementation of an impedance calculation algorithm is proposed. The algorithm structure is developed and successfully integrated into an FPGA including a high-level control unit. Through initial tests the basic functionality and accuracy of the embedded algorithm is shown. The influence of the embedded algorithm on detectability and resulting increase of system safety is discussed. The developed system sets the baseline for further investigations and online data gathering in deployed systems by providing an adaptable measurement solution for impedance values.

6. Outlook

Future research will focus on extended verification and data gathering with usage of this algorithm. A battery analysis board is currently in development which will use this algorithm as a base to execute fully autonomous impedance measurements. Correlations with monitored effects will be performed. This might lead to an extended impedance interpretation functionality of the impedance analyzer.

Acknowledgements

The research was conducted in the center for mechatronic systems (ZMS) of the University Aalen in cooperation with the Advanced Mechatronics GmbH. The Author wants to thank all employees for the helpful feedback and work that contributed to this publication.

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