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Miniaturization of Phase-Difference-of-Arrival Based Visible Light Positioning Receiver Using Field Programmable Gate Arrays

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Miniaturization of indoor visible light positioning (VLP) receiver plays a key role in advancing VLP towards practical usage. However, the current phase-difference-of-arrival (PDOA) algorithm for VLP is both time-consuming and power-hungry computing for an embedded system. In this paper, a low-complexity PDOA algorithm for VLP and its implementation on field programmable gate arrays (FPGA) board is presented. Considering the actual computing capability of embedded system, a low-complexity PDOA algorithm is designed. With the support of Xilinx design suite, an FPGA-based firmware is implemented to locate users by sequential means of 1) obtaining analog-digital converter signal 2) filtering and demodulation of signals using FPGA device for PDOA measurements of low-complexity. Last but not the least, a microprocessor is adopted to receive the PDOA estimation from FPGA chip for further trilateration and hence providing the positioning results. A real-time hardware-in-the-loop (HIL) simulation has been carried out to evaluate the feasibility and performance of the proposed embedded VLP receiver in term of its accuracy and real-time performance. The results successfully validated the proposed embedded VLP receiver using PDOA algorithm of low complexity.

1. Introduction

Indoor positioning has stronger and stronger demand, especially with emergence and rapid development of industrial internet-of-things (IIoT). However, both global navigation satellite system (GNSS) and cellular networks which are well-validated in outdoor scenario hardly deliver satisfying accuracy for indoor positioning. Indoor environment can cause several problems to affect the position estimation accuracy [1]. The main problems are the multipath transmission and attenuation caused by the complicated indoor environment, which degrade the performance of the system and hence reduce the positioning accuracy significantly while signals passing between transmitter and receiver [2]. Therefore, researchers paid increased attention to other spectrum than radio frequency domain, for example the optical wireless channel [3]. As such, the domain of visible light positioning (VLP) has undergone substantial advancements in the recent 5 years.

Likewise, many techniques which have been employed for the radio frequency spectrum wireless indoor localization are applied to VLP, such as Received Signal Strength (RSS) [4,5] and Time-Difference-of Arrival (TDOA) [6]. Although using RSS for VLP is the easiest approach and able to achieve higher accuracy than radio frequency spectrum wireless indoor localization, the accuracy boundary is not easy to lift due to that RSS approach is still sensitive to the multipath effect and attenuation. As per our previous research work [7-9], TDOA approach and its variants phase-difference-of-arrival (PDOA) approach provide better accuracy than RSS. However, high complexity of current PDOA algorithm for VLP results in time-consuming and computing-power-hungry for an embedded system implementation, which hinders the miniaturization of PDOA-based VLP receiver.

To address this challenge, VLP system using adapted PDOA algorithm is proposed in this paper. In order to ensure the embedded system can estimate the PDOA of input signals in a fast and light way, the algorithm is optimized in terms of signal preprocessing and filter adoption.

The contribution of this paper is twofold. Firstly, to our best knowledge, we for the first time report the miniaturization of PDOA-based VLP via modularized PDOA process. Secondly, an adapted PDOA algorithm friendly for computation-power-constrained embedded device is proposed also for the first time.

The remaining part of this paper is organized as follows. In Section 2, the proposed PDOA algorithm adapted to embed system is presented and the implementation on the Field programmable gate arrays (FPGA) is also explained. Section 3 describes the real-time hardware-in-the-loop (HIL) simulation to prove the feasibility and study the performance, following by results discussion. Finally, the conclusions are summarized in Section 4.

2. Design and theory

2.1 Embedded PDOA-based VLP receiver

The block diagram of the embedded VLP receiver for PDOA is shown in Fig. 1. Considering the actual computing capability of embedded system and the desired computation speed of the miniaturization design, the PDOA estimation process is proposed to be modularized and allocated to FPGA and ARM processor based on their competency. The various components include photodetector, analog-digital convertor (ADC), FPGA-based high-speed processor, microchip control unit (MCU) and Raspberry-Pi-based high

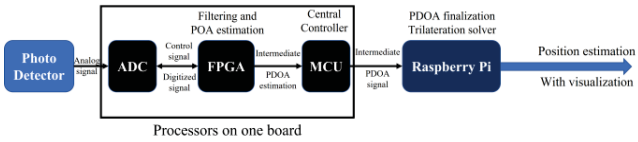

Fig. 1 Components of the embedded receiver of PDOA-based VLP performance processor.

The embedded VLP receiver is designed in such a way that it co ordinates with LED beacons which are slightly modified from comme rcially available LED lightings by intensity modulation of carrier sign al. Furthermore, photodetector in the VLP receiver collects the intensi ty of carrier signal from the LED beacons within the field of view. Ph otodetector passes the AC of light intensity to ADC for processing an d removes the DC of light intensity for illumination. Then, ADC sam ples or digitizes the analog signal detected by the photodetector. ADC would wait for the control signals from the FPGA to start/stop the di gitization and handover the digitized signal through a serial protocol. Subsequently, the digital signals would be pre-processed by the FPGA in a fast manner. The process includes filtering and partially measuri ng the PDOA of signal. MCU next to FPGA, which is a low-cost 8-bi t microcontroller, acts as the data transmission bridge which connects the FPGA and the subsequent Raspberry-Pi-based high-performance processor. At both sides data transmission would be based on the seria l protocol. The remaining calculation of PDOA would be performed b y the high-performance processor, i.e., 32-bit ARM based Raspberry Pi. The remaining PDOA measurement comprises of division and tan gent functions which FPGA is not good at. Apart from that, Raspberry Pi will also execute the numerical solution of the position estimation from the trilateration equation after the PDOAs are obtained and eve ntually visualize the position estimation.

2.2 Low-complexity PDOA algorithm in FPGA

Novel PDOA algorithm is adapted for embedded system to achieve low complexity and save hardware resources by minimizing the usage of filters. The algorithm is aimed to be implementable on an embedded system integrating FPGA with Raspberry Pi. The procedure of algorithm inside FPGA includes buffering the ADC output, pre-processing by high-pass filtering, first peak finder and truncation, I/Q multiplication with VLO, low-pass filtering by averaging. After that, extraction of phase information and position estimation inside Raspberry Pi based on hyperbolic trilateration just follows the state-of-art works.

2.2.1 Buffering the ADC output

ADC task would be activated by sending the clock signal from FPGA to ADC chip. FPGA stops the ADC automatically by terminating the enable signal when the buffering RAM is full which would be indicated by the address signal from RAM. Digitized signal is assumed to contain the carrier signals irradiated from the 1st ~m^{th} LED and DC noise η_D as well as other noise term η. Let the frequency of carrier irradiated by i-th LED be f_i, sampling rates be Sp, initial phase be ϕ_i, time-of-flight from i-th LED to the receiver be t_i, t_{trun} be the shift time caused by signal truncation due to start/stop of ADC, we have the digitized signal S(n) given by,

$$S(n) = \sum_{i=1}^{m} \sin\left(2\pi f_i \cdot \left(\frac{n}{Sp} + t_i + t_{trun}\right) + \phi_i\right) + \eta_D + \eta \quad (1)$$

2.2.2 Pre-processing by high-pass filtering

Original noise in DC components will greatly affect the extraction of correct phase information since the phase information is moved to DC components from high frequency ones. It is necessary to lower the noise in DC components by applying the high pass Filter at the beginning. After filtering, S(n) can be rewritten as,

$$S(n) = \sum_{i=1}^{m} \sin\left(2\pi f_i \cdot \left(\frac{n}{Sp} + t_i + t_{trun}\right) + \phi_i\right) + \eta \quad (2)$$

2.2.3 First peak finding and truncation

The term t_{trun} must be ensured that it is equal to integer multiples of common period of carrier 1st ~m^{th} each time we sample the received signal so that the effect from term t_{trun} on the phase calculation would be avoided. There are various ways to achieve this. The way we opt for herein for explanation is to truncate the data into the one starting from the signal peak. In this way, t_{trun} can be offset as $2\pi f_i \cdot t_{trun} = N \cdot 2\pi$ after peak finder and truncation. Hence,

$$S(n) = \sum_{i=1}^{m} \sin\left(2\pi f_i \cdot \left(\frac{n}{Sp} + t_i\right) + \phi_i\right) + \eta \quad (3)$$

The true value of peak location will be found recursively by comparing with the data while incrementing the address. The procedure of finding the peak is concluded as below.

1. Initialize variable *addr*=0, which is corresponding to address signal from buffering RAM signal (i.e., n in S(n)).
2. Store the value of S(*addr*) to variable tmp_{pk}, create and initialize another variable $Addr_{pk}$.
3. Increments *addr*, compare S(*addr*) with tmp_{pk}; If S(*addr*)> tmp_{pk}, Refresh tmp_{pk} as S(*addr*) and $Addr_{pk}$ as *addr*.
4. Check if *addr* has reached the maximum value of RAM address: if so terminated, otherwise, repeat step 3.

The location the peak of the mixed sinewave within the first common period is found and stored in variables of $Addr_{pk}$. According to the *addr* corresponding to peak $Addr_{pk}$, abandon the data from n=1 to n=$Addr_{pk}$. Eventually, the truncation of data is completed.

2.3.4 I/Q multiplication

I/Q multiplication with virtual local oscillator (VLO) [9] is applied to move phase/time information onto DC frequency component. For each frequency f_i, two virtual local signals from VLO are given by,

$$L_{i,1}(n) = \sin\left(2\pi f_i \cdot \frac{n}{Sp}\right) \quad (4)$$

$$L_{i,2}(n) = \sin\left(2\pi f_i \cdot \frac{n}{Sp} + \frac{\pi}{2}\right) \quad (5)$$

The I/Q multiplication for each frequency f_i is performed so as to acquire t_i.

$$I_i(n) = S(n) \cdot L_{i,1}(n) = \left[\sum_{j=1}^{m} \sin\left(2\pi f_j \cdot \left(\frac{n}{Sp} + t_j\right) + \phi_j\right) + \eta\right] \cdot \sin\left(2\pi f_i \cdot \frac{n}{Sp}\right). \quad (6)$$

If we denote $\left[\sum_{j=1, j\neq i}^{m} \sin\left(2\pi f_j \cdot \left(\frac{n}{Sp} + t_i\right) + \phi_i\right) + \eta\right] \cdot \sin\left(2\pi f_i \cdot \frac{n}{Sp}\right)$ as IC_{hf} which has no DC frequency component, I_i can be rewritten as,

$$I_i(n) = \sin\left(2\pi f_i \cdot \left(\frac{n}{Sp} + t_i\right) + \phi_i\right) \cdot \sin\left(2\pi f_i \cdot \frac{n}{Sp}\right) + IC_{hf}. \quad (7)$$

Furthermore, we have

$$I_i(n) = -\frac{1}{2}\left[\cos\left(2\pi \cdot 2f_i \cdot \frac{n}{Sp} + 2\pi f_i t_i + \phi_i\right) - \cos(2\pi f_i \cdot t_i + \phi_i)\right] + IC_{hf}. \quad (8)$$

Likewise for $Q_i(n)$,

$$Q_i(n) = -\frac{1}{2}\left[\cos\left(2\pi \cdot 2f_i \cdot \frac{n}{Sp} + 2\pi f_i t_i + \phi_i + \frac{\pi}{2}\right) - \cos\left(2\pi f_i \cdot t_i + \phi_i - \frac{\pi}{2}\right)\right] + QC_{hf}, \quad (9)$$

where

$$QC_{hf} = \left[\sum_{j=1, j\neq i}^{m} \sin\left(2\pi f_j \cdot \left(\frac{n}{Sp} + t_i\right) + \phi_i\right) + \eta\right] \cdot \sin\left(2\pi f_i \cdot \frac{n}{Sp} + \frac{\pi}{2}\right). \quad (10)$$

Evidently, t_i can be extracted by applying low-pass filtering onto $I_i(n)$ and $Q_i(n)$ as described in the next step.

2.3.5 Low-pass filtering by averaging

Low-pass filtering can be realized in several ways. Here, averaging method is being used to realize the low-pass filtering for convenience of easy explanation. Realization of low-pass filtering using averaging method is both light and fast, reducing the algorithm complexity significantly. With low-pass filtering applied onto I_i and Q_i, we have

$$\begin{cases} MeanI_i = \frac{\sum Q_i(n)}{\sum n} = \frac{1}{2}\cos(2\pi f_i \cdot t_i + \phi_i) \\ MeanQ_i = \frac{\sum I_i(n)}{\sum n} = \frac{1}{2}\sin(2\pi f_i \cdot t_i + \phi_i) \end{cases}. \quad (11)$$

In this way, the phase/time information is attained by removing other unrelated components. The rest operation of extracting phase information followed by calculating TDOA and positioning just used the same process in [9], which is easy for the Raspberry Pi on the embedded system to handle.

3. HIL Simulation

3.1 HIL simulation setup

HIL Simulation is used herein to simulate the performance in the ideal scenarios in real-time. Complex embedded systems would be tested using the HIL simulation technique. As shown in Fig. 2, the ideal scenario would be considered in which three LED beacons would be placed at the specific coordinates in the cartesian system. The coordinates of three LED beacons are (0.375, 0.210), (0.710, 0.792), (1.125, 0.210), respectively, in the unit of meter. Three LEDs would be all mounted with height of 2 m. RF carrier frequency assigned to LED1, LED2, LED3 is 4.8 MHz, 5 MHz, and 5.2 MHz respectively. In this scenario, simulated ADC input signal, local signals are provided as inputs to the processor of embedded VLP receiver in the HIL simulation. Since the simulated ADC signal used here is an ideal signal, HPF and truncation process is not required. Consider a real time scenario in which the experiment would be done with coverage area of 2×2 m^2 which contains 9 position coordinates.

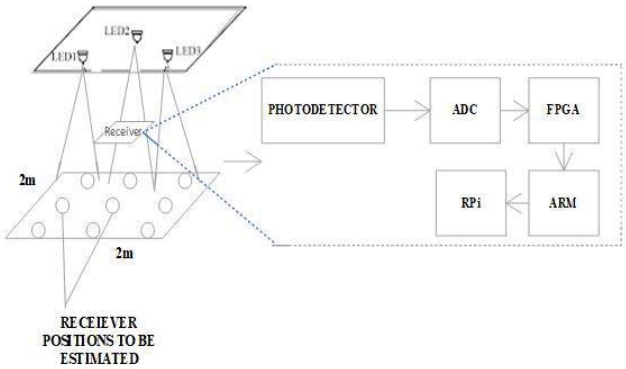

Fig. 2 Scenario simulated by HIL testing in real-time

In the HIL simulation, for each position coordinate, respective ADC input signal would be given as the input to FPGA (Spartan LX150). ADC input signals for each position coordinate would be obtained using MATLAB and pre-stored in input ROM of FPGA using COE file. Then FPGA program will process the input signals as explained in the principle section. User would visualize the results by another terminal or monitor remotely and wirelessly connected to the raspberry pi. Fig. 3 depicts the prototype of the embedded PDOA-based VLP estimator at the receiver side, which is as compact as a mouse.

As the user console, Raspberry Pi application obtained the TDOA results from FPGA and perform the positioning, providing plot of the original position coordinates and estimated position coordinates to determine the positioning error.

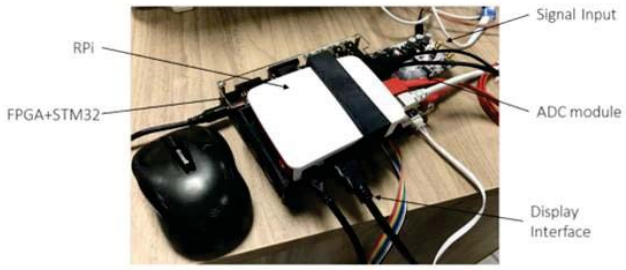

Fig. 3 Prototype of embedded PDOA-based VLP receiver

3.2 HIL simulation results and discussion

Total of nine different positions across the coverage area were estimated by providing respective ADC input signals to the FPGA. Moreover, the results under sampling rates of 50 MSa/s and 51.2 MSa/s were both studied and compared.

The plot provided by Raspberry Pi under sampling rate of 51.2 MSa/s is shown in Fig. 4. In general, the estimated positioning is very close the actual positions. The rate of positioning is measured up to 3 Hz on such a computation-constrained device.

Results obtained for the sampling rate of 51.2 MSa/s and 50 MSa/s are further summarized in Tab. 1. As per Tab. 1, the average positioning error under 51.2 MSa/s is 0.018 m, while the average positioning error under 50 MSa/s is up to 0.449 m. It is evident to

conclude that positioning errors with the sampling rate of 50 MSa/s are much worse compared to the positioning errors with sampling rate of 51.2 MSa/s. This is due to that the positioning accuracy highly depends on the optimal combination of data length and the sampling rate being used. Hence, the combination of the data length and the sampling rate should be chosen wisely such that the complete cycle of input signal should be acquired during the process of sampling or digitization. With the combination of sampling rate of 50 MSa/s and data length as 512, the data is not in multiples of signal periods during the process of sampling, hence results in poor averaging results leading to bad positioning accuracy. Whereas in combination of sampling rate of 51.2 MSa/s and data length as 512, complete cycles of input signal have been acquired in the process of sampling which results in higher positioning accuracy.

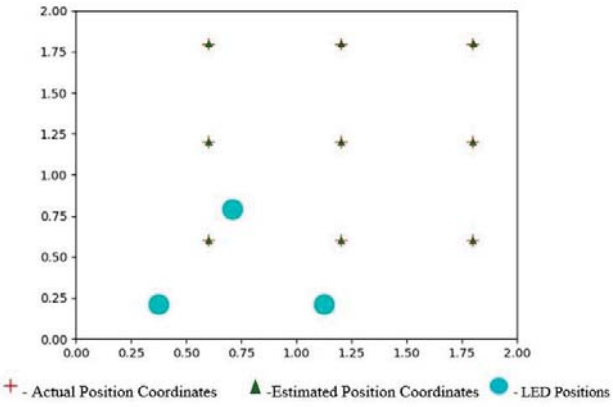

Fig. 4 Plot of positioning results for sampling rate of 51.2 MSa/s

Estimated coordinates (m)	Actual coordinates (m)	Positioning error (m) using Sampling rate of 50 MSa/s	Positioning error (m) using Sampling rate of 51.2 MSa/s
(0.59, 0.6)	(0.6, 0.6)	0.5025	0.01
(1.17, 0.6)	(1.2, 0.6)	0.305	0.03
(1.78, 0.6)	(1.8, 0.6)	0.707	0.02
(0.58, 1.18)	(0.6, 1.2)	0.53	0.028
(1.18,1.19)	(1.2,1.2)	0.6	0.022
(1.79, 1.2)	(1.8, 1.2)	0.78	0.01
(0.6, 1.79)	(0.6, 1.8)	0.62	0.01
(1.17, 1.79)	(1.2, 1.8)	0.73	0.03
(1.79, 1.8)	(1.8, 1.8)	1.08	0.01

Tab. 1 Positioning error under different sampling rate

4. Conclusions

In this paper, we have implemented a VLP receiver on an embedded device based on the adapted PDOA algorithm of low complexity to cater for the constrained computing capability in the miniaturization design. an FPGA-based firmware is designed to implement the adapted PDOA algorithm, while a microprocessor is adopted to receive the PDOA estimation from FPGA chip for further trilateration and hence providing the positioning results. HIL simulations have been performed on the proposed embedded VLP receiver based on real time scenarios to test the accuracy and processing speed. The HIL simulation indicates a superior performance, specifically, the positioning error is 0.018 m in an ideal scenario covering a 2×2 m^2 area when the distance from the LED transmitter and the receiver is about 2 m.

In future, the designed VLP system in future should be fully experimentally tested with real signals from photodetectors receiving the modulated signals from LED lightings. Secondly, Data length employed in our HIL simulation is only 512, and positioning accuracy of the VLP system can be further improved by increasing the length of the data to be processed with optimal combination of sampling rate.

ACKNOWLEDGEMENT

REFERENCES

1. Luo, J, Fan L. and Li H., "Indoor positioning systems based on visible light communication: state of the art." IEEE COMMUNICATONS SURVEYS & TUTORIALS, Vol. 19, No. 4, pp. 2871-2893, 2017
2. Lin, B., Tang X., Ghassemlooy Z., Lin, C. and Li Y., "Experimental demonstration of an indoor VLC positioning system based on OFDMA." IEEE Photonics Journal, Vol. 9, No. 2, pp. 1-9, 2017.
3. Rahman, A., Li T. and Wang, Y., "Recent Advances in Indoor Localization via Visible Lights: A Survey." Sensors, Vol. 20, No. 5, pp. 1382, 2020.
4. Chen, H., Han W., Wang, J., Lu, H., Chen, D., Jin, J. and Feng, L., "High accuracy indoor visible light positioning using a long-short term-memory fully connected network-based algorithm." Optics Express, Vol. 29, No. 25, pp. 41109-41120, 2021.
5. Tran, H. Q. and Ha, C., "Improved Visible Light-Based Indoor Positioning System Using Machine Learning Classification and Regression." Applied Sciences, Vol. 9, No. 6, pp. 1048-1072, 2019.
6. Kazikli, E. and Gezici, S., "Hybrid TDOA/RSS based localization for visible light systems." Digital Signal Processing, Vol. 86, pp. 19-28, 2019.
7. Zhang, S., Du, P., Chen, C., Zhong, W. and Alphones, A., "Robust 3D Indoor VLP System Based on ANN Using Hybrid RSS/PDOA." IEEE Access Vol. 7, pp. 47769-47780, 2019.
8. Zhang, S., Zhong, W., Du, P. and Chen, C., "Experimental demonstration of indoor sub-decimeter accuracy VLP system using differential PDOA." IEEE Photonics Technology Letters, Vol. 30, No. 19, pp. 1703-1706, 2018.
9. Du, P., Zhang, S., Chen, C., Alphones, A., and Zhong, W., "Demonstration of a low-complexity indoor visible light positioning system using an enhanced TDOA scheme." IEEE Photonics Journal, Vol. 10, No. 4, pp. 1-10, 2018.