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Investigation on the Characteristic of Plasma De ep Etching in Wafer Cutting Industry

Kuan-Yu Lin[1,2,#], Jia-Jhih Shen[1], Chia-Hao Chang[1], Chih-Hung Liu[1], Ta-Hsin Chou[1] and Keh-Chyang Leou[2]

1 Mechanical and Mechatronics System Research Laboratories, Industrial Technology Research Institute, Taiwan
2 Department of Engineering and System Science, National Tsing Hua University, Taiwan
Corresponding Author / E-mail: guanyulin@itri.org.tw

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In response to the demand of component function enhancements, through silicon via technology for 3D IC package, wafer thinning and dicing and micro-electromechanical systems deep film etching process, the traditional etch processes will face a lot of challenges. The process examination of a vacuum plasma equipment system for silicon wafer dicing process has been discussed in this study. The experimental platform is inductively couple plasma (ICP) etching equipment built by ITRI MMSL to carry out the etching process of 12 inch silicon wafer. In this research, the influence of some important plasma parameters on the etching rate of silicon wafer has been explored, including that of ICP source power, radio frequency (RF) bias power, etching gas flow rate and process pressure. The 11.4 μm/min etching rate of the patterned wafer can be achieved by our design of the experiment with our etching equipment. It is found that when the SF_6 flow rate increases, there are more etching species in the plasma, and the higher of RF bias power, the positive ions in the plasma are easily accelerated by the electric field in the vertical direction. Therefore, the ions can easily bombard the surface of the silicon wafer for physical etching, then the etching rate can be improved. The results of this study can be used to be parameter requirements of subsequent deep reactive ion etching processes in the future work.

NOMENCLATURE

ICP = Inductively coupled plasma
CCP = Capacitively coupled plasma
RIE =Reactive ion etch
DRIE = Deep reactive ion etch
3D IC = Three-dimensional integrated circuit
2D IC = Three-dimensional integrated circuit
MEMS = Micro electro mechanical system
TSV= Through silicon via
SCCM=Standard cubic centimeter per minute

1. Introduction

DRIE has been the most popular and actively developed dry plas ma etching technology in the optoelectronic and semiconductor fields recently. It has excellent anisotropic etching, high depth and high asp ect ratio etching characteristics. In the new generation of MEMS man ufacturing and 3D IC and other industrial development. It takes on a k ey deep etching process technology that promotes the re-upgrade of hi gh-end electronic products.

MEMS have become the main driving force for the continuo us progress and transformation of mobile wearable, automotive e lectronics and medical device markets [1].

In the other hand, response to recent years, the semiconductor industry has gradually faced many technical difficulties and challenges in the 2D scale integration circuit, including component design and physical limits of semiconductor processes and equipment. The emerging 3D IC process and packaging technology has become the main trend of the future development of the semiconductor industry. All the 3D IC chips in the vertical direction are connected with TSV technology [2].

Therefore, TSV is nothing more than the most important link in the 3D IC manufacturing and packaging process. Here, the core technology used is the DRIE process. However, the stability and precision of the TSV technology also bring significant challenges to the performance and yield of 3D IC process and packaging.

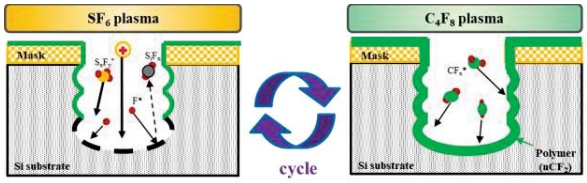
2. Applications of Plasma Deep Etching Technology

2.1 Plasma Deep Etching Technology

With the advancement of process technology, traditional etching technology has been unable to achieve DRIE applications. In order to

meet the special silicon etching conditions, the deep etching technology (Bosch process) developed by Robert Bosch, Germany. The Bosch process is all plasma processes are mainly composed of etching and passivation, and a high aspect ratio deep etch profile is accomplished by cyclically alternating between the two procedures. As shown in Fig. 1, the passivation procedure uses the C_4F_8 gas. The C_4F_8 gas will generate active radicals of fluorocarbon species (such as CF_x*) in the plasma environment and conducts the polymer deposition reaction.

This thin film is also called a protective layer or a passivation laye r, which can protect the trench sidewalls from being over-etched durin g the etching process and maintain the verticality of the trench profile. The etching process mainly uses the SF_6 etching gas. The SF6 etching gas decomposes in the plasma environment to produce positive ion groups (S_xF_y+) and reactive radicals (F*) and other species.



Etching	Passivation
Ex : $SF_6 + e^- \rightarrow S_xF_y^+ + S_xF_y^* + F^* + e^-$ $Si + F \rightarrow SiF_x\uparrow$ (volatile gas)	Ex : $C_4F_8 + e^- \rightarrow CF_x^+ + CF_x^* + F^* + e^-$ $CF_x^* \rightarrow nCF_2$ (polymer)

Fig. 1 The basics of the bosch process

2.2 Plasma Deep Etching Equipment

With the continuous progress and improvement of semicondu ctor process technology. The ICP reactive ion etching has been developed with high plasma density and low process pressure. T he electromagnetic field effect is enhanced by special induction coil equipment, which can generate high-density plasma at lower working pressure. Due to the reduced probability of ion collisi on, better anisotropic etching can be obtained, and the high den sity plasma can also effectively improve the etching rate [4].

Compared with the traditional CCP-RIE etching system, the ICP-RIE etching system can achieve a high etching rate and hig h aspect ratio etching effect (Fig. 2).

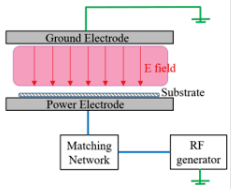
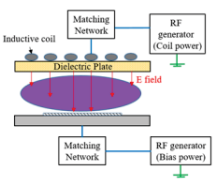
System type	CCP-RIE	ICP-RIE
Image		
Plasma density (ion/cm³)	10^9~10^{11}	10^{10}~10^{12}
Work pressure (mtorr)	100 ~1000	0.5~50
Etching rate (μm/min)	< 1	3~5 (even more)
Anisotropy	worse	better (90±1°)
Aspect ratio	< 10:1	> 20 : 1

Fig. 2 Comparison of CCP-RIE and ICP-RIE Etching Systems

3. The Results of Plasma Deep Etching Process

3.1 The Equipment Architecture in This Study

The architecture of the ICP-RIE etching system established in this research is shown in Fig. 3. It is mainly composed of a cavity with vacuum and other related components, such as Dry Pump, Turbo Pump, 13.56 MHz RF Power, Electrostatic chuck, Vacuum pressure gauges, Mass flow meter control system and other components. The maximum allowable wafer size is 12 inch (Ø300 mm), and the wafer placement method is manual placement. When the RF current passes through the coil, an alternating magnetic field is generated, and then an electric field is generated through inductive coupling. In a low pressure state, the gas can be ionized and collisional to generate a high density plasma.

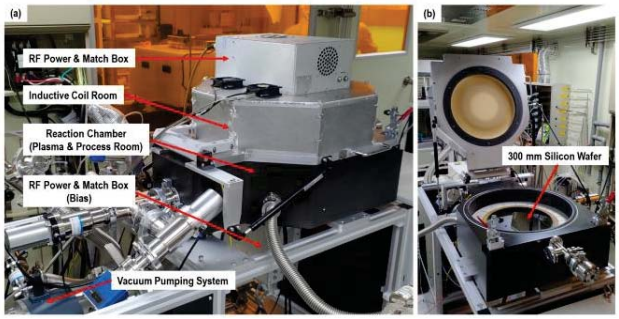


Fig. 3 (a) Plasma Etching Machine; (b) For 12 inch silicon wafer

3.2 The Results of Design of Experiments for The Silicon Wafer Etching Process

When using SF_6 plasma for silicon wafer etching process verification, it is necessary to consider that the main gas phase dissociation reaction in SF_6 plasma is

$$e + SF_{6(g)} \xrightarrow{k_{7-x}} SF_{x-1(g)} + F_{(g)} + e \quad (x = 3\sim6)$$

Among them, SF_x and F atoms are the etching reaction species of silicon material, and their etching reaction with the surface of Si wafer is

$$4F_{(g)} + Si \rightarrow SiF_{4(g)}$$

$$4SF_{x(g)} + Si \rightarrow SiF_{4(g)} + 4SF_{x-1(g)} \quad (x = 3, 5)$$

In this study, the wafer surface has strip patterns with diffe rent line widths of 30, 50, 70, 90, 110, 130, 150, and 170 μm, respectively. The silicon wafer surface has a photoresist layer (0.5 μm) and a hard mask layer (SiO_2 = 2 μm) from top to bo ttom. The actual sample and structure are shown in Fig. 4. In t he main process, SF_6 gas is used to etch the silicon wafer and the L15 orthogonal arrays is established according to the experi mental design method. Experiments #2, #14, and #15 were expe rimented under the same conditions, in order to observe the repr oducibility of the process. All process times are 3 min and the process parameters of each factor refer to the integrated table in Table 1, and define the operating range of 3 levels: ICP power (1000 W, 1500 W, 2000 W), SF_6 gas flow (50 SCCM, 100 S

CCM, 150 SCCM), bias power (0 W, 30 W, 60 W) and distrib uted in the orthogonal arrays as shown in Table 1.

After the silicon wafer is etched, it can be converted into a n etching rate after being measured by a film thickness tester (α -step). The experimental results are listed in the right column of Table 1, and the factor effect analysis is shown in Fig. 5.

In the factor effect results of this study, it can be found th at when the SF_6 flow rate is increased, the etching species in th e plasma are more (F), and a higher concentration of etching sp ecies can effectively increase the etching rate of silicon wafers. When the bias power is higher, the positive ions in the plasma are easily accelerated by the electric field in the vertical directio n, so that the ions can easily bombard the surface of the silicon wafer for physical etching, which increases the etching rate.

In the current experiment, #9 has the highest etching rate, which is about 8.26 μm/min and conforms to the trend of the factor effect.

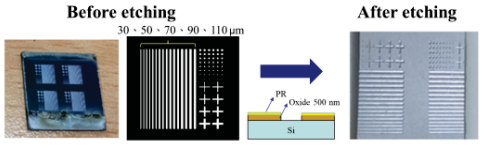


Fig. 4 The pattern and structure of the test silicon wafer

Table 1 The orthogonal arrays and etch rate results for the design of experiment

	Source power (W)	SF_6 flow rate (SCCM)	Bias power (W)	Etch rate (μm/min)
#1	2000	100	0	6.44
#2	1500	100	30	6.86
#3	2000	50	30	3.91
#4	2000	100	60	7.28
#5	1500	50	0	4.09
#6	1000	100	60	4.66
#7	1500	150	60	7.54
#8	1500	150	0	6.04
#9	2000	150	30	8.26
#10	1500	50	60	3.73
#11	1000	150	30	4.06
#12	1000	50	30	3.68
#13	1000	100	0	3.4
#14	1500	100	30	6.34
#15	1500	100	30	5.49

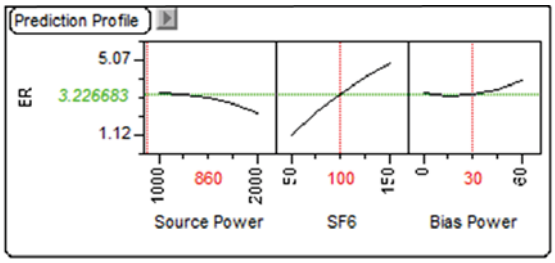


Fig. 5 The silicon wafer etch rate of factor effect diagram

3.3 The Results of Photoresist Patterned Silicon Wafer Etching

In this subsection of the study, we used the photoresist patte rn on a silicon wafer (shown in Fig. 6) for the etch process val idation. There are three main groups of process conditions, as s hown in Table 2. We changed the SF_6 gas flow rate, ICP powe r and Bias power respectively, to discuss the effect of different operating parameters on silicon etching of speed. The etching re sults were measured using a surface profiler (α-step) to analyze the etching depth and converted into etching rate. The results ar e shown in Fig. 7.

We compare the etching results obtained under different process c onditions. Fig. 7 (a) shows that since the electrostatic chuck doesn't a pply bias power, the ions bombarded on the wafer surface have no en ergy, just only plasma potential energy.

In Fig. 7(b), when the ICP plasma power is increased to 15 00 W and the bias power is set at 65 W, due to the increase i n the plasma density, the ion flux reaching the wafer surface in creases, and there is a certain amount of bombardment energy, t hen the etch rate increases significantly. At this time, the etchin g mechanism is mainly RIE, and its etching rate is much higher than the pure chemical etching reaction.

The process conditions of Fig. 7(c) are mainly to increase th e flow rate of the SF_6 gas and the power of the ICP. Compare d with FIG. 7(b), due to the increased plasma density and disso ciation into etching reactive species, neutral radicals and ions. A lthough the bias power is the same as the ion bombardment ene rgy, the etch rate can also be greatly increased from 3 μm/min to 11.4 μm/min.

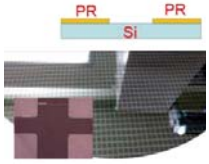


Fig. 6 The photoresist pattern of a silicon wafer

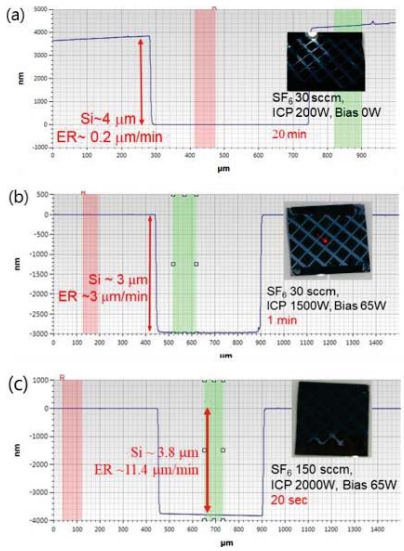


Fig. 7 Different operating conditions and the etch depth measure ment results of the surface profilers. (a) etch time 1,200 sec; (b) etch time 60 sec; (c) etch time 20 sec

Table 2 The process operating conditions for a photoresist pattern of a silicon wafer

	(a)	(b)	(c)
SF_6 flow rate	50 SCCM	30 SCCM	150 SCCM
ICP power	200 W	1500 W	2000 W
Bias power	0 W	65 W	65 W
Etch time	1200 sec	60 sec	20 sec
Etch rate	0.2 μm/min	3 μm/min	11.4 μm/min

3.4 The Results of Deep Etching BOSCH Process

The deep etch BOSCH process uses a patterned silicon wafer as a test sample is shown in Fig. 4. In this study, the deep etching process was carried out by the Bosch process. The SF_6 etching reaction and the C_4F_8 deposition reaction were repeated three times. The detailed process parameters are shown in Table 3.

It can be observed that there are different etch depths for different line widths, the etch depth distribution from wide to narrow ranges from about 21.6 μm to 35.1 μm, and the etch rate is about 1.5 to 2.3 μm /min. It is speculated that the exposed Si of the wider track is more, so that the reaction time required for etching species is longer and the etch rate is also slower.

The etching profiles of all line widths are mainly bowl-shaped structures and the current process parameters are mainly isotropic etching. Due to the high process pressure, the species concentration is also high, causing more etching species to perform Si etching reaction by diffusion and collision mechanism. Therefore, more etched species have a higher chance of colliding with the sidewall to react, resulting in a more obvious side etching phenomenon.

Table 3 The parameter conditions for the etching and deposition processes

Etching Process Parameters			
ICP power	2000 W	Pressure	120 mTorr
Bias power	65 W	Etching Time	5 mins
SF_6	150 SCCM		
Deposition Process Parameters			
ICP power	2000 W	Pressure	110 mTorr
Bias power	-	Deposition Time	2 mins
C_4F_8	100 SCCM		

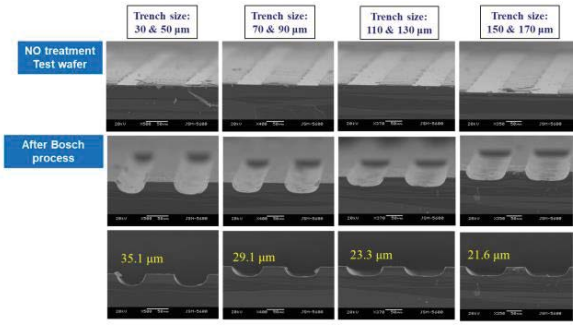


Fig. 8 The four kinds of trench size cross-sectional SEM features after the etching process through the ICP

4. Conclusions

In this study, the plasma stability and etching process tests of a plasma etching machine have been completed. We discuss the influence of important process parameters such as ICP power, bias power and working pressure on the etching rate of silicon wafers through the design of experiments method. Then, to obtain the best etching process parameters as the benchmark parameter settings for the wafer dicing. At present, the verticality of the etched sid ewalls in the etching process has not been well controlled. The etching and deposition process parameters still need to be adjust ed to achieve an etching profile with better verticality. In the fu ture, it can be combined with plasma emission spectroscopy and radio frequency ion diagnostic systems to improve the accuracy of the process.

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REFERENCES

1. T. Xu, Z. Tao, H. Li, X. Tan and H. Li, "Effects of deep reactive ion etching parameters on etching rate and surface morphology in extremely deep silicon etch process with high aspect ratio", Advances in Mechanical Engineering, Vol. 9, No. 12, p. 168781401773815, 2017.
2. I. Abhulimen, S. Polamreddy, S. Burkett, L. Cai and L. Schaper, "Effect of process parameters on via formation in Si using deep reactive ion etching", Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, Vol. 25, No. 6, p. 1762, 2007.
3. H. Jansen, M. de Boer, S. Unnikrishnan, M. Louwerse and M. Elwenspoek, "Black silicon method: X. A review on high speed and selective plasma etching of silicon with profile control: an in-depth comparison between Bosch and cryostat DRIE processes as a roadmap to next generation equipment", Journal of Micromechanics and Microengineering, Vol. 19, No. 3, p. 033001, 2009.
4. F. Marty, L. Rousseau, B. Saadany, B. Mercier, O. Français, Y. Mita and T. Bourouina, "Advanced etching of silicon based on deep reactive ion etching for silicon high aspect ratio microstructures and three-dimensional micro- and nanostructures", Microelectronics Journal, Vol. 36, No. 7, pp. 673-677, 2005.