

Exploration of optimate surface roughness of plasma-based atom-selective etching process of single-crystal silicon

Bing Wu¹, Hui Deng^{1,#}

¹ Department of Mechanical and Energy Engineering, Southern University of Science and Technology, No. 1088, Xueyuan Road, Shenzhen, Guangdong, 518055, China
Corresponding Author / Email: dengh@sustech.edu.cn (H. Deng)

KEYWORDS: Single-crystal silicon, atomic-scale polishing, plasma etching, roughness, oxide

Single crystal silicon (Si) is the most widely used material in the electronic industry. The atomic-scale smooth surface of Si is important for advancing quantum electronics and X-ray optics. In our previous study, to realize the damage-free, highly efficient, and atomic-level polishing of single-crystal Si, plasma-based atom-selective etching (PASE) was proposed. According to the mechanism of PASE, an atomic-scale ultrasmooth Si surface with well-arranged two dangling bonds could be obtained theoretically. In this work, optimization of plasma etching parameters was conducted to further explore the optimate surface roughness of Si. Plasma diagnostics were conducted to investigate the plasma temperature and composition of radicals. The effects of RF power, the flow rate of reactive gases, work distance, and irradiation time on the optimate surface roughness of PASE for Si were investigated. A ground Si (100) surface was smoothed to the roughness below 0.15 nm over 10 μm^2 by PASE within 2 min. This optimate surface roughness is better than that of conventional CMP, in which a S_a roughness of 0.3 nm can be obtained. However, it was found that the thin oxide layer on the Si surface affected the surface roughness, hindering further reduction of roughness. Overall, this study has shown the potential of PASE for achieving atomic-scale ultrasmooth surface of Si. Also, better surface roughness is assumed to be achievable if appropriate vacuum systems without post-PASE oxidation or contamination are adopted.

NOMENCLATURE

Si = silicon
CMP = chemical mechanical polishing
CARE = catalyst-referred etching
PASE = plasma-based atom-selective etching
MRR = material removal rate
ACSM = atomic and close-to-atomic scale manufacturing
ICP = inductively coupled plasma

1. Introduction

Single-crystal silicon (Si) is the most widely used semiconductor material in the electronics industry [1]. Planarization of Si substrates is an important process for semiconductor devices and optical elements. For these applications, atomic-scale smooth surfaces of Si are strongly required, such as quantum devices, extreme ultraviolet, and X-ray optics [2,3]. The chemical mechanical polishing (CMP)

method is generally used to polish the Si surface, which modified the surface based on slurry and then removed the modified layer using soft abrasives. Ultrasmooth Si surface can be obtained with the S_a roughness lower than 0.4 nm [6]. However, the material removal rate (MRR) was low and the use of abrasives inevitably induced unwanted mechanical attacks [7]. An abrasive-free polished method using catalyzed chemical etching, catalyst-referred etching (CARE), has been developed. Atomic-smooth SiC surface without subsurface damage has been achieved [8]. However, the MRR is on the order of nm/h [9,10].

Recently, to realize the high efficiency, atomic-level and damage-free polishing of Si, plasma-based atom-selective etching (PASE) was proposed [11]. Through the selective removal of Si atoms with more dangling bonds under high temperatures, only Si atoms with two dangling bonds will be well arranged to keep the surface ultrasmooth theoretically. Therefore, the optimate surface roughness of the PASE process was investigated in this study, which is of great significance for the development of atomic and close-to-atomic scale manufacturing (ACSM) [12,13]. Optimization

of parameters was conducted to explore the optimum roughness. It was found that the thin oxide layer on the Si surface hinders further reduction of roughness.

2. Experimental setup

Fig. 1 shows the schematic diagram of the PASE setup. The platform was mainly composed of a radio frequency (RF) power supply, a network matcher, an electric sparker, an inductance coil, a quartz torch, and four mass flow controllers. The flow rates of the gases were controlled by the mass flow controllers. The quartz torch contains inner and outer tubes. The inner tube contains the gaseous reactants, CF_4 and O_2 , which are combined with the carrier gas argon (Ar) for plasma ignition. A high flow rate of Ar flowed into the outer tube to cool the inner tube and shield the plasma from the ambient air. The sparker is used for pre-breakdown of the gas to generate more electrons for promoting the plasma ignition. A plasma was generated by applying a 27.12-MHz RF power on the inductance coil. The matcher was used to match the impedance to maximize the forward RF power. The Si substrate was mounted on a 3-axis NC platform.

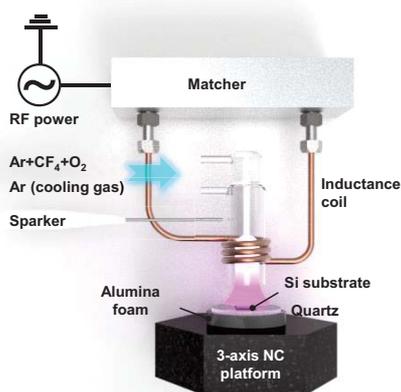


Fig. 1 Schematic diagram of the experimental setup

Commercially available Si wafers with p-type doping, the orientation of (100), were used in this study. The initial surface was polished by CMP. The pre-processed surface roughness was shown in Fig. 4 (a) and (b). The wafers were cut into slices with dimensions of $10 \times 10 \text{ mm}^2$. The Si substrates were ultrasonically cleaned in ethyl alcohol and deionized water for 5 min. The plasma temperature was confirmed by the infrared thermal camera (FLIR T660). The composition of radicals and density were determined by optical emission spectroscopy (OES, Ocen optics USB4000). The roughness was measured by atomic force microscopy (AFM, Bruker Edge). The thickness of the oxide layer on the Si surface was measured by ellipsometry.

3. Plasma diagnostics

According to the mechanism of PASE, high temperature and high

density of the etching radicals are essential for polishing Si [11]. Thus, plasma diagnostics were conducted. Fig. 2(a) shows the temperature curve during PASE polishing within 2 min under 700 W. When the RF power was turned on, the temperature immediately rose to about $1000 \text{ }^\circ\text{C}$ in the first 20 s. Then, the temperature increased slowly to $1168.5 \text{ }^\circ\text{C}$. Once the RF power was turned off, the temperature of plasma slowly dropped to room temperature. The inset shows a typical thermal infrared image of the wafer during PASE. This high-temperature property of atmospheric inductively coupled plasma (ICP) enables enlarging the etching rate difference between the Si atoms with different dangling bonds [11].

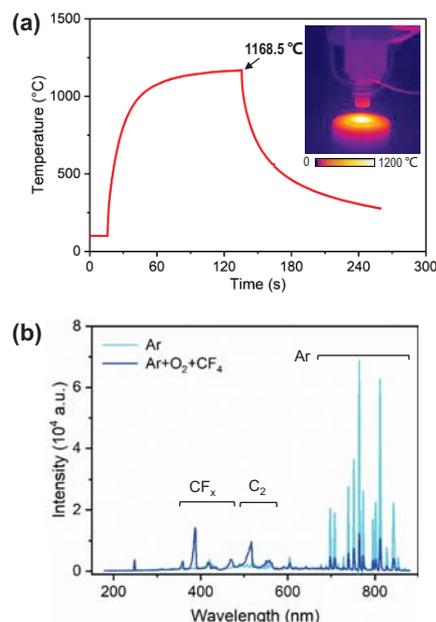


Fig. 2 Plasma diagnostics of PASE. (a) Temperature curve during polishing under 700 W (inset shows the infrared thermal image); (b) Optical emission spectra of the inductively coupled plasma torch with the Ar(1.5 slm), and O_2 (20 sccm), CF_4 (60 sccm).

Fig. 2(b) shows the optical emission spectra of the plasma. When no reactive gases, CF_4 and O_2 , were added, only the peaks corresponding to the de-excitation of Ar atoms were detected. While in PASE etching mode, strong peaks corresponding to CF_x and C_2 radicals were generated [14]. These radicals were dissociated from CF_4 , proving the generation of F atoms [15]. The spectra indicate the high concentration of active radicals in the ICP torch, which is necessary to achieve efficient polishing of silicon. The high-temperature and high density of radicals are the key features that distinguish the atmospheric ICP from traditional low-temperature vacuum plasma [16].

4. Results and discussions

To explore the optimum surface roughness of PASE, optimization of the key parameters during the etching process was conducted. The input RF power, the CF_4/O_2 ratio, the torch-wafer distance, and

etching duration play important roles in the PASE process, which affect the radical density and etching temperature. The polishing duration of Fig. 3(a), (b), and (c) was constant at 2 min. The Sa roughness was measured in the area of $10 \times 10 \mu\text{m}^2$ in Fig. 3. As shown in Fig. 3(a), the surface roughness was firstly decreased and then increased with the increase of RF power from 550 W to 700 W. The thickness of the oxide on the Si surface has the same trend as the roughness. The etching temperature increases nearly linear with the

increase of RF power. From 550 W to 600 W, the Sa roughness decreased due to the increasing temperature. However, the temperature further increased induced thermal oxidation, which hindered the further reduction of roughness with the RF power. Fig. 3(b) shows the variation of Sa roughness with the flow rate of CF_4 while keeping other conditions constant strictly. The roughness of all Si substrates was below 0.2 nm and had no obvious relationship with the CF_4 flow rate.

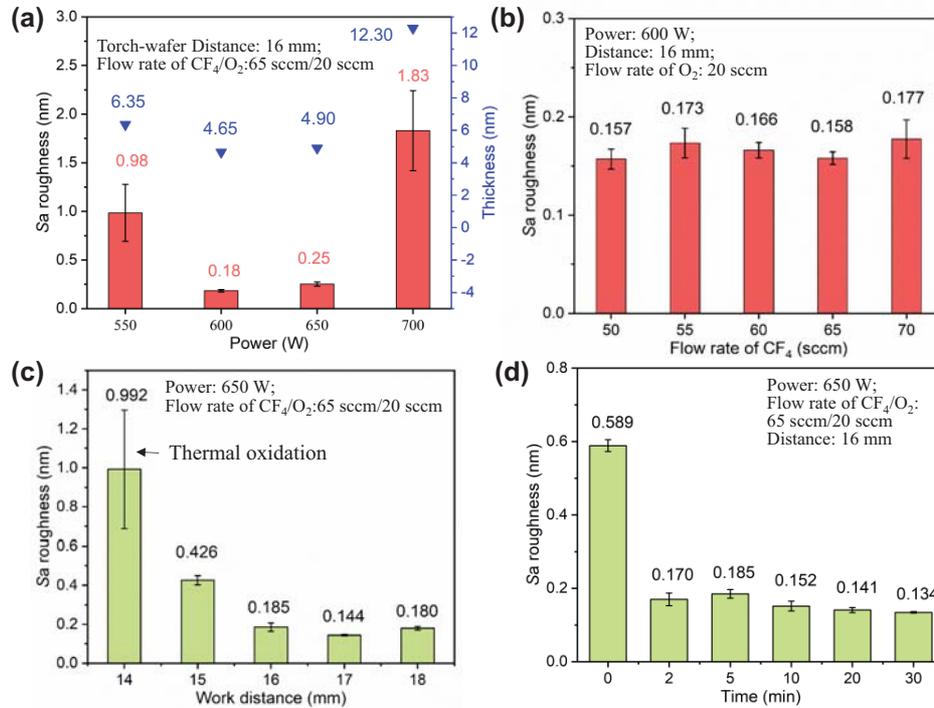


Fig. 3 The effect of RF power, the flow rate of CF_4 , work distance, and polishing duration (a-d) on surface Sa roughness. The error bar represents the standard deviations of multiple measurements.

Fig. 3(c) shows the correlation between the Sa roughness with torch-wafer distance. With the distance increased from 14 to 18 mm, the Sa roughness reduced from 0.992 to 0.144 nm at 17 mm and then increased to 0.18 nm at 18 mm. The temperature decreased with the increase of torch-wafer distance. When the distance was 14 mm, the high temperature induced thermal oxidation. Therefore, the roughness decreased with the extent of oxide. However, the further reduced temperature resulted in the roughness increased when the distance was 18 mm. Fig. 3(d) shows the variation of Sa roughness with PASE duration. After PASE-processed for 2 min, the roughness was reduced from 0.589 to 0.170 nm quickly. With the polishing time increased to 30 min, the roughness reduced slowly to 0.134 nm. It indicates that the roughness is almost at its limit. Therefore, by optimizing these key parameters, the atomic-smooth surface roughness of 0.134 nm can be obtained.

As shown in Fig. 2, the plasma temperature is quite high in PASE, so Si is very susceptible to oxide after this thermal process. Fig. 4 shows the AFM images of the pre-processed and PASE-processed Si surfaces. In contrast to the surface showing a high degree of roughness and multiple scratches before PASE processing, the PASE-processed surface was very smooth with a roughness of 0.132

nm. Fig. 4(d) shows some island-like protuberances, which may be the oxide on the surface [17]. The roughness increased on both the surface and the interface in the initial oxidation stage and tends to saturate for thicker regions [17,18]. These SiO_2 islands resulted in a deterioration in the surface and interface roughness. Therefore, it can be concluded that the thin oxide layer induced by the thermal process hindered further reduction of optimum roughness of PASE. Theoretically, better surface roughness is assumed to be achieved according to the mechanism of PASE [11].

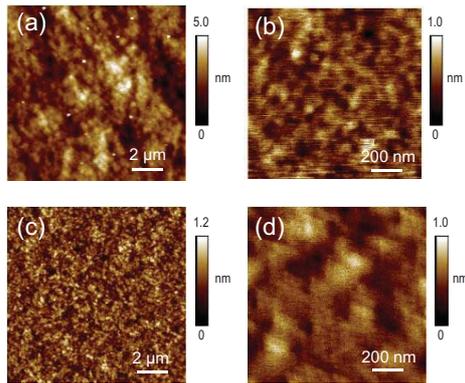


Fig. 4 AFM images of the (a) $10 \times 10 \mu\text{m}^2$ area (S_a : 0.572 nm) and (b) $1 \times 1 \mu\text{m}^2$ area of the CMP-processed Si surface (S_a : 0.185 nm). AFM image of the (c) $10 \times 10 \mu\text{m}^2$ area of PASE-processed Si surface (S_a : 0.132 nm) and (d) $1 \times 1 \mu\text{m}^2$ area (S_a : 0.122 nm).

5. Conclusions

This extended abstract has presented the potential for atomic and close-to-atomic scale manufacturing of PASE. Plasma diagnostics demonstrated the properties of high temperature and large radical density of atmospheric ICP. Under the optimized conditions, an atomically smooth surface with a roughness of 0.132 nm was obtained. However, owing to the thermal interaction of PASE, oxide of Si was easy to occur. The AFM image showed the oxide island, which increase the surface roughness and masked the atomically smooth interface after PASE treatment.

In future works, high-resolution transmission electron microscopy (HRTEM) will be conducted to further investigate the Si/SiO₂ interface and subsurface of the PASE-processed Si. To further confirm oxidative deterioration of roughness caused by the thermal process in PASE, other processes will be introduced to remove surface oxide.

REFERENCES

- [1] G. Fisher, M.R. Seacrist, R.W. Standley, Silicon crystal growth and wafer technologies, *Proc. IEEE*, 100 (2012) 1454-1474.
- [2] S. Goswami, K. Slinker, M. Friesen, L. McGuire, J. Truitt, C. Tahan, L. Klein, J. Chu, P. Mooney, D.W. Van Der Weide, Controllable valley splitting in silicon quantum devices, *Nat. Phys.*, 3 (2007) 41-45.
- [3] H. Yumoto, H. Mimura, T. Koyama, S. Matsuyama, K. Tono, T. Togashi, Y. Inubushi, T. Sato, T. Tanaka, T. Kimura, Focusing of X-ray free-electron laser pulses with reflective optics, *Nat. Photonics*, 7 (2013) 43-47.
- [4] Z.J. Pei, G.R. Fisher, J. Liu, Grinding of silicon wafers: A review from historical perspectives, *Int. J. Mach. Tool Manufact.*, 48 (2008)

1297-1307.

- [5] M. Forsberg, Effect of process parameters on material removal rate in chemical mechanical polishing of Si (1 0 0), *Microelectron. Eng.*, 77 (2005) 319-326.
- [6] J. Li, Y. Liu, Y. Dai, D. Yue, X. Lu, J. Luo, Achievement of a near-perfect smooth silicon surface, *Sci. China Technol. Sci.*, 56 (2013) 2847-2853.
- [7] L. Zhang, I. Zarudi, Towards a deeper understanding of plastic deformation in mono-crystalline silicon, *Int. J. Mech. Sci.*, 43 (2001) 1985-1996.
- [8] H. Hara, Y. Sano, H. Mimura, K. Arima, A. Kubota, K. Yagi, J. Murata, K. Yamauchi, Damage-free planarization of 4H-SiC (0001) by catalyst-referred etching, in *Mater. Sci. Forum, Trans Tech Publ*, 2007, pp. 749-751.
- [9] D. Toh, P. Van Bui, K. Yamauchi, Y. Sano, Photoelectrochemical oxidation assisted catalyst-referred etching for SiC (0001) surface, *Int. J. Auto. Tech.*, 15 (2021) 74-79.
- [10] T. Okamoto, Y. Sano, H. Hara, T. Hatayama, K. Arima, K. Yagi, J. Murata, S. Sadakuni, K. Tachibana, Y. Shirasawa, Reduction of surface roughness of 4H-SiC by catalyst-referred etching, in: *Mater. Sci. Forum, Trans Tech Publ*, 2010, pp. 775-778.
- [11] Z. Fang, Y. Zhang, R. Li, Y. Liang, H. Deng, An efficient approach for atomic-scale polishing of single-crystal silicon via plasma-based atom-selective etching, *Int. J. Mach. Tool Manufact.*, 159 (2020) 103649.
- [12] F. Fang, Atomic and close-to-atomic scale manufacturing: perspectives and measures, *Int. J. Extrem. Manuf.*, 2 (2020) 030201.
- [13] P. Wang, J. Wang, F. Fang, Study on Mechanisms of Photon-Induced Material Removal on Silicon at Atomic and Close-to-Atomic Scale, *Nanomanuf. Metrol.*, 4 (2021) 216-225.
- [14] R. d'Agostino, F. Cramarossa, S. De Benedictis, G. Ferraro, Spectroscopic diagnostics of CF₄- O₂ plasmas during Si and SiO₂ etching processes, *J. Appl. Phys.*, 52 (1981) 1259-1265.
- [15] T. Jung, D. Kim, H. Lim, Molecular emission of CF₄ gas in low-pressure inductively coupled plasma, *Bull. Korean Chem. Soc.*, 27 (2006) 373-375.
- [16] S. Tachi, K. Tsujimoto, S. Okudaira, Low- temperature reactive ion etching and microwave plasma etching of silicon, *Appl. Phys. Lett.*, 52 (1988) 616-618.
- [17] K. Ohsawa, Y. Hayashi, R. Hasunuma, K. Yamabe, Roughness increase on surface and interface of SiO₂ grown on atomically flat Si (111) terrace, in: *J. Phys. Forum, IOP Publ*, 2009, pp. 012031.
- [18] A. Carim, R. Sinclair, The evolution of Si/SiO₂ interface roughness, *J. Electrochem. Soc.*, 134 (1987) 741.